

METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS (MOSFETS) USED IN INK-JET HEAD CHIPS AND METHOD FOR MAKING THE SAME

BACKGROUND OF THE INVENTION

Field of Invention

5 The invention relates to a MOSFET and the method for manufacturing them. In particular, it relates to a MOSFET for ink-jet heads and the associated manufacturing method.

Related Art

10 The inkjet printer ejects ink droplets on a printing medium to form desired texts or pictures. The size, shape, material, density, and positioning of the produced ink droplets are important factors that will affect the printing quality. The smaller the ink droplet size is, the higher printing resolution one can achieve. However, under normal conditions, the printing speed is also sacrificed. In order to promote the printing speed and resolution, the number of nozzles on the print head chip is the substantial solution.

15 To achieve this objective, driving devices with switch and active characteristics such as transistors and the ink droplet actuators are often integrated into a single inkjet print head chip. The number of cartridge contact points X and the number of nozzles Y are promoted from the one-to-one driving mode ($X=Y$) to one-to-many mode ($Y=(X/2)^2$). Such integrated driver head (e.g. ejecting ink droplets using thermal bubbles) is normally made by connecting
20 a metal oxide semiconductor field effect transistor (MOSFET) with a droplet actuating thermal resistor in series. A sufficiently high driving current has to pass through the MOSFET at a voltage around 10V for the thermal bubble actuator to obtain enough energy to generate bubbles that eject ink droplets out. Since the MOSFET used in the inkjet print head chip is used under large currents and voltages, it is commonly to use with phosphosilicate
25 glass (PSG) for the 1st interlayer dielectric. The temperature is raised to be higher than 1000

°C to drive the phosphor within the PSG into silicon, forming the N⁺ diffusion of source and drain with deep junctions. The junction depth is about 1.2 μm to 1.8 μm. In addition to avoiding the spiking at the Al-Si contact surface, the N⁺ diffusion with deep junction can increase the breakdown voltage of the MOSFET. With the increase of the printing speed and resolution, using tiny ink droplets and increasing the inkjet frequency have become the primary objectives. Consequently, the energy required to form each individual ink droplet gets lower. The needed current and voltage also decreases accordingly. At the same time, the line width required by the MOSFET is made thinner to increase the device density on a chip. In summary, these requirements of inkjet print head chips have made the existing driving device structure and specification are not satisfactory.

SUMMARY OF THE INVENTION

To make MOSFET's that satisfy high package density requirements for the inkjet print head chips, the invention provides a MOSFET used in ink-jet head chips and the corresponding manufacturing method. A silicon substrate is formed with a source and a drain with a shallower doped junction depth. A process in lower temperature is used to achieve the requirements for making print head chips with a high device density.

To achieve the above objective, the disclosed MOSFET contains an active region and a body-contact active region on the silicon substrate. A gate insulator is grown across the active region. Polysilicon is then deposited on the insulating layer to form the gate of the MOSFET. A source and a drain are defined in the active region by diffusion or ion implantation. The active region and the gate are partially covered by borophosphosilicate glass (BPSG), which is formed with a reflow treatment. Places on the BPSG that corresponding to the source and the drain are formed with contact holes, filled with a plug material to prevent the spiking of the contact between aluminum and silicon at the drain during subsequent processes. To increase the device density, the gate length is between 0.35 μm and 3.5 μm. The depth sum of the junction at the source and the drain is 0.2 to 0.75 times the gate length.

The chip of the integrated-driver head is formed by combining the above-mentioned MOSFET device, an actuator, and an ink-flow structure. The MOSFET device is in electrical communications with the actuator. The voltage on the gate controls the current flowing through the actuator. The ink-flow structure contains ink channels, ink-firing chambers and
5 nozzles that allow ink to pass through. The actuator is connected with the ink-flow structure to provide the energy for ink to be ejected out of the nozzles.

More explicitly, the disclosed method for making MOSFET's used in the printhead with high-density devices contains the steps of: defining in order an active region and a gate on the silicon substrate, with the gate length ranging from $0.35\mu\text{m}$ to $3.5\mu\text{m}$; doping impurities on
10 both sides of the gate to form a drain and a source, with the junction depth of the drain dopant being 0.1 to 0.6 times the gate length; and covering the active region and the gate with reflowed BPSG, which has contact holes filled with a plug material at the drain positions.

Said BPSG has a thickness ranging from 150nm to 1000nm, a boron content between 0.5 wt% and 6.0 wt%, and a reflow temperature between 850°C and 925°C . The plug material
15 has a thickness between $0.01\mu\text{m}$ and $1.0\mu\text{m}$, and a material selected from the group consisting of W, Pt, Ti, Co, Ni, Mo, Ta, Si, and their alloys or compounds.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will become more fully understood from the detailed description given hereinbelow illustration only, and thus are not limitative of the present invention, and
20 wherein:

FIGS. 1 to 7 are the manufacturing flowcharts in an embodiment of the invention; and

FIG. 8 is a schematic view of the chip in the disclosed integrated drive head.

DETAILED DESCRIPTION OF THE INVENTION

With reference to FIGS. 1 to 7, we use the n-channel metal oxide semiconductor field

effect transistor (nMOSFET) as an example to explain the procedure of an embodiment of the invention. First, a silicon substrate is performed with the process of local oxidation of silicon (LOCOS), forming a field oxide (FOX) and defining out an active region and a body-contact active region. As shown in FIG. 1, the silicon substrate 10 is oxidized to form a stress buffer oxide 11. It is further deposited with a silicon nitride 12 using the chemical vapor deposition (CVD) method. After lithography and etching steps, the active region and the body-contact active region are defined on the silicon nitride 12. As shown in FIG. 2, a thick FOX 13 is subsequently formed using high-temperature wet oxidation. Finally, the stress buffer oxide 11 and the silicon nitride 12 are removed, forming the structure in FIG. 3.

Secondly, the gate is defined and the active region is doped to form a drain and a source. For different threshold voltages, a screen oxide is first formed and implanted with boron as the threshold voltage implantation. Afterwards, the screen oxide is removed. As shown in FIG. 4, a gate oxide 14 with a thickness range from 10 nm to 75nm is formed by oxidation at high temperatures and then deposited with polysilicon to form a gate. Finally, a polysilicon gate 16 is defined by lithography and etching. The gate 16 has a thickness range from 0.1 μ m to 0.4 μ m and a length L range from 0.35 μ m to 3.5 μ m.

The next step is doping the source 18 and the drain 17. As shown in FIG. 5A, phosphor (P) or phosphide is doped on both sides of the gate 16 by ion implantation or diffusion to form an n-doped junction as a drain 17 and a source 18. The dopant depth is 0.1 to 0.35 that of the gate length. If the shallow junction is needed, arsenic (As) or arsenide may be used as the dopant. One may also choose to use As, P and their compounds simultaneously to form an n-doped junction. Moreover, to increase the drain breakdown voltage and to reduce n-doped encroaching under gate, the drain can be doped with drain-side-only phosphor dopant to form a deeper but low-concentration n^- -doped junction 19, as shown in FIG. 5B. The next step is to dope the drain 17 and the source 18 to be a shallower but high-concentration n^+ -doped junction. The goal is to have the doped junction depth of the drain 17 greater than the

junction depth of the source 18. The depth of the n^- -doped junction 19 of the drain 17 is about 0.1 to 0.6 times the gate length. The final doped junction depth sum of the source 18 and the drain 17 is 0.2 to 0.75 times the gate length.

5 After doping the source 18 and the drain 17, the body-contact active region is defined with a base doping region 21 to perform p-type doping (see FIG. 6). The first step is to deposit a low-temperature undoped silicon oxide (LTO, not shown), followed by depositing BPSG on its surface. The BPSG is reflowed as a first interlayer dielectric layer 20. The thickness range of undoped LTO is from 20nm to 250nm; the thickness range of the BPSG is from 100nm to 1000nm. The reflow-temperature range of the BPSG is from 850°C to 925°C. The lower
10 reflow temperature can prevent too deeper dopant driven-in at the source 18 and the drain 17. As shown in FIG. 7, contact holes are formed at the drain 17, the source 18 and the body-contact 21. If the MOSFET has shallower source and drain junctions, the plug material filling the contact holes can prevent the spiking between aluminum and silicon at the source and the drain.

15 The disclosed integrated-driver head chip has a structure formed using the above-mentioned MOSFET. With reference to FIG. 8, a thermal-resistor layer 22 and a first conductive layer 23 is formed and defined upon the substrate. They are then covered by an insulating layer 24 and a passivation layer 25. The insulating layer 24 has some via 31 connecting to the first conductive layer 23 for providing electrical connect between the first
20 conductive layer 23 and a second conductive layer 27. One can form an intermetal barrier 26 under the second conductive layer by evaporation or sputter. The intermetal barrier 26 can enhance the adhesion of the contact points between the chip and the circuit board. Finally, a thick photo resist 29 is used to define the ink-flow channels and the ink firing chamber 28. The ink-flow architecture is completed after bonding with a nozzle plate 30.

25 Certain variations would be apparent to those skilled in the art, which variations are considered within the spirit and scope of the claimed invention.